

A cross-sectional view of a semiconductor device. A gate electrode (15) is positioned on top of a gate oxide layer (16). The gate electrode is connected to a GATE CONTACT (17). The device features two source/drain regions (13a and 13b) which are N+ type, embedded in a P-type substrate (12a and 12b). These regions are separated by a central channel region (12c1 and 12c2). The source/drain regions are connected to SOURCE & BODY CONTACT (18) and DRAIN CONTACT (19). The device is mounted on a substrate (10) with a dashed line (11) indicating an interface. Arrows (20a and 20b) point to the source/drain regions. Other labels include 9, 15, 16, 18, 19, 12a, 12b, 12c1, 12c2, N+, N-, and 10.

[illegible]

A cross-sectional view of a semiconductor device. A gate electrode 19 is positioned on top of a gate oxide layer 35. The gate oxide layer 35 is on a substrate 11. The substrate 11 has a P- region 20a and an N- region 20b. A source/body contact 18 is connected to the P- region 20a. A gate contact 17 is connected to the gate electrode 19. The device includes a channel region 21a and a drain region 21b. The channel region 21a is formed in the P- region 20a. The drain region 21b is formed in the N- region 20b. The channel region 21a is separated from the drain region 21b by a channel stop 22c1. The drain region 21b is separated from the channel region 21a by a drain stop 22c2. The device is connected to a source/body contact 18 and a gate contact 17.

FIG._4a

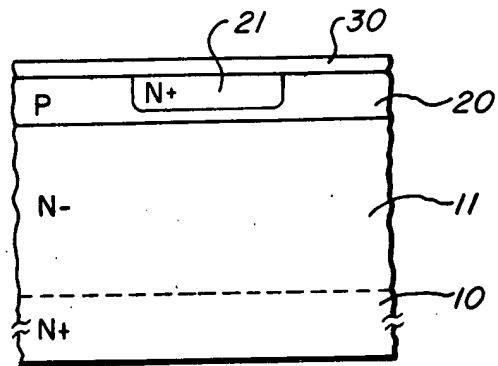


FIG._4b

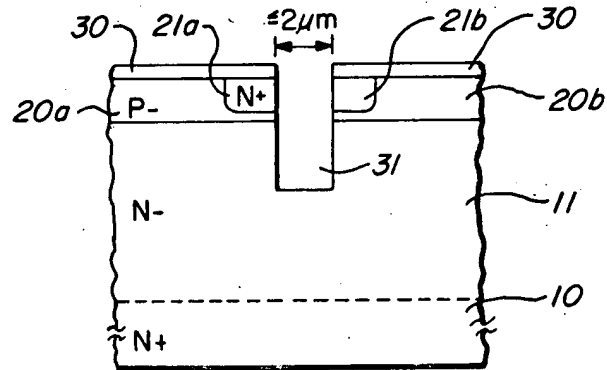


FIG._4c

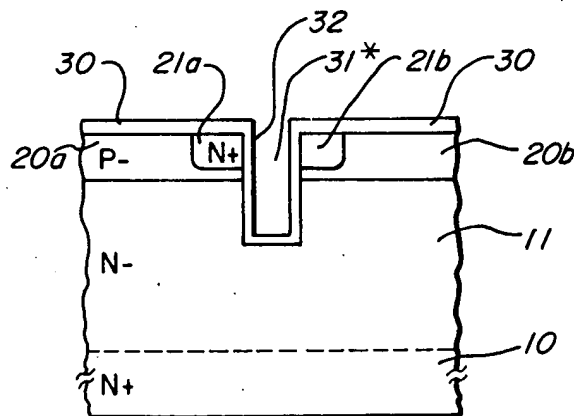


FIG. 4d

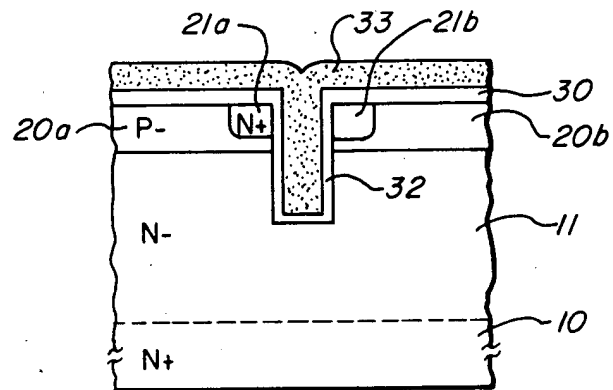


FIG. 4e

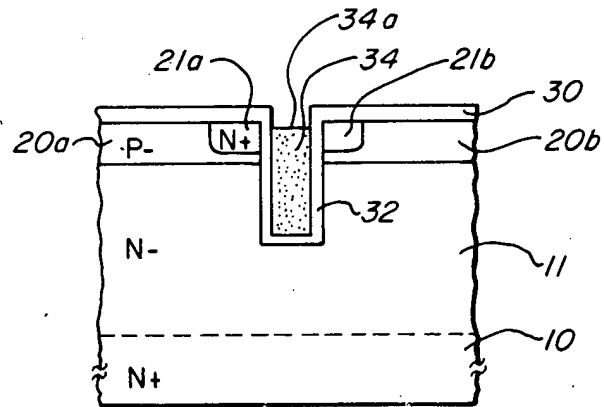


FIG. 4f

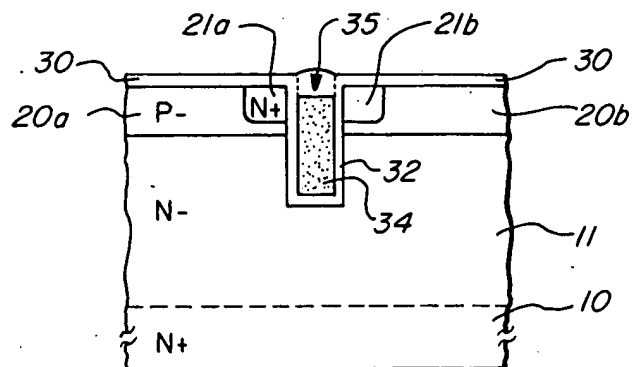


FIG._5

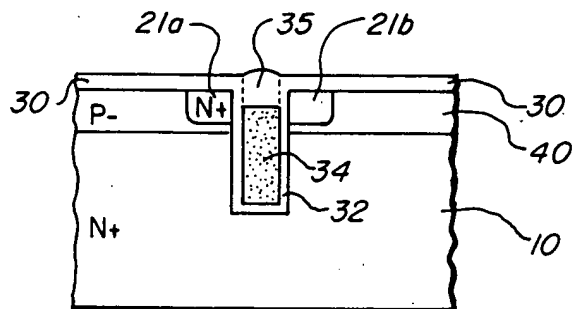


FIG._6

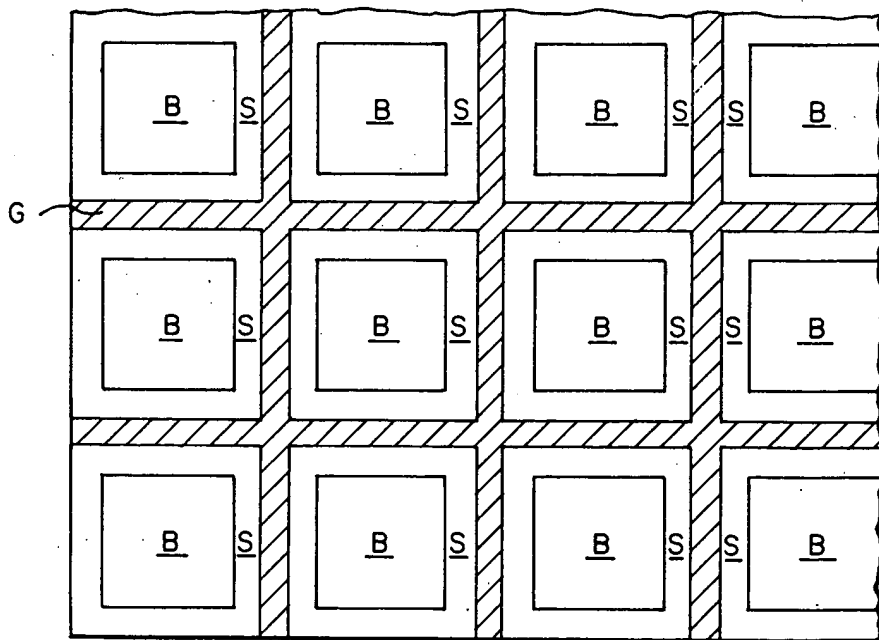
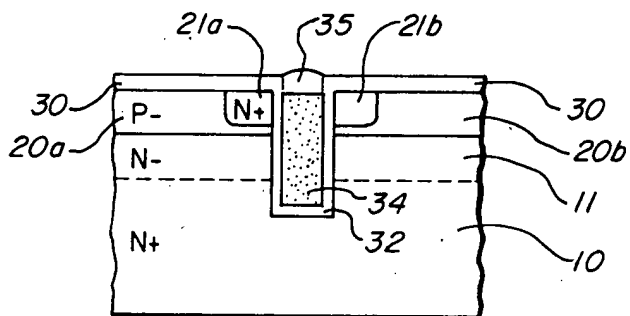
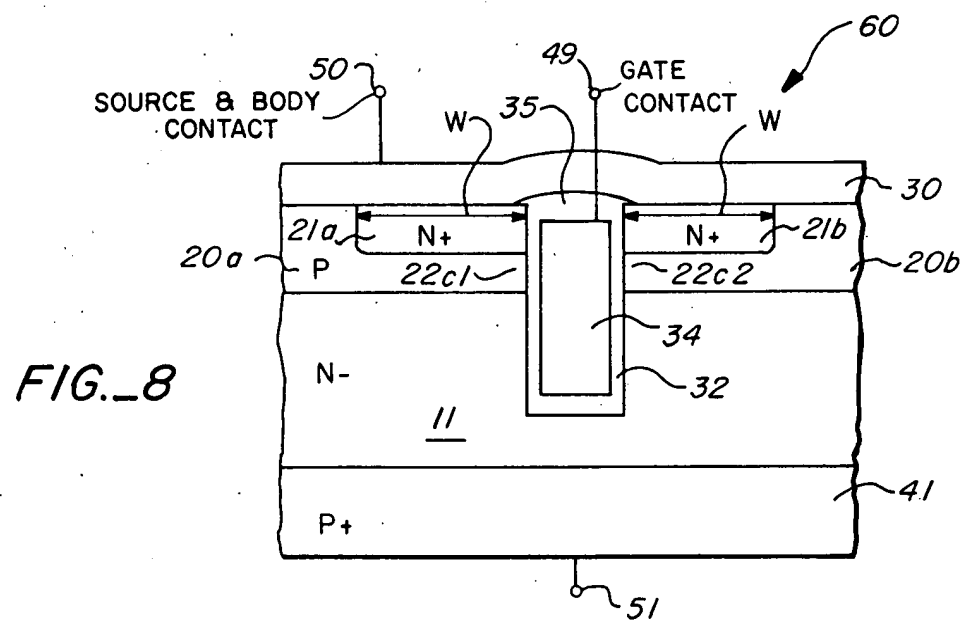
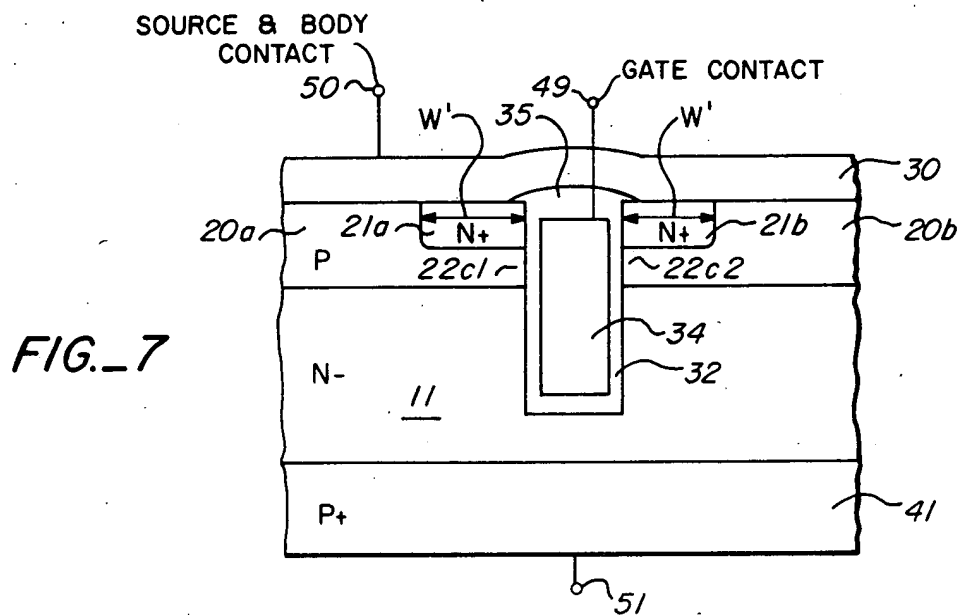


FIG._9



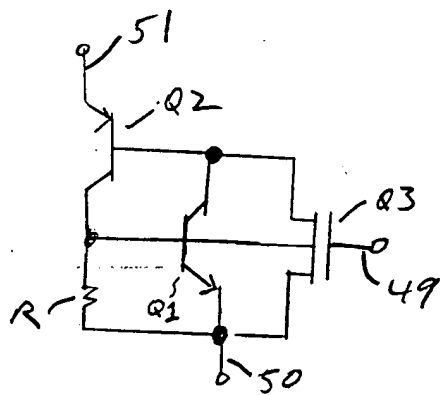


FIG. A